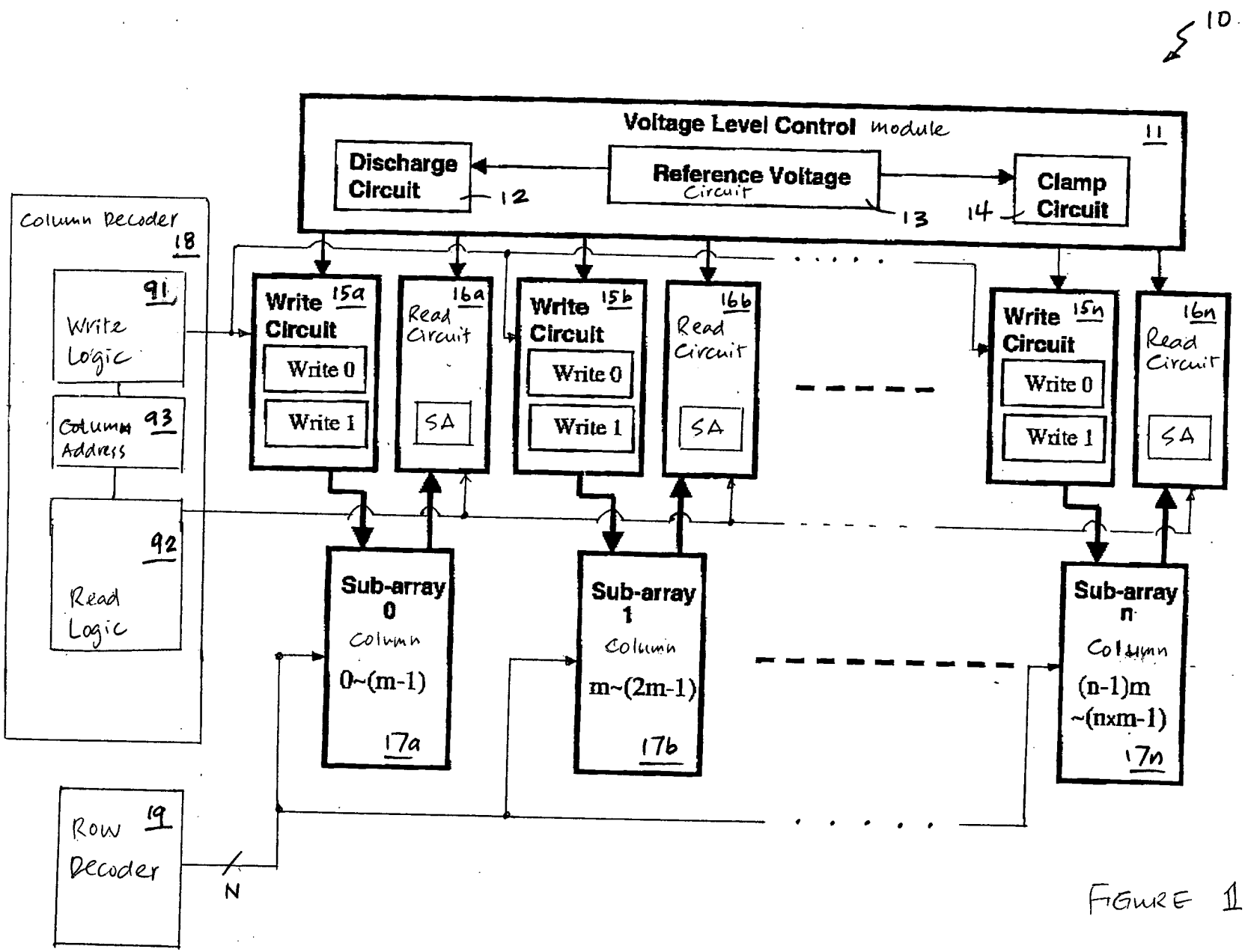
10
Voltage Level Control module
11
Discharge Circuit
12
Reference Voltage Circuit
13
14
Clamp Circuit
Column Decoder
18
91
Write Logic
93
Column Address
92
Read Logic
Write Circuit
15a
Write 0
Write 1
Read Circuit
16a
SA
Write Circuit
15b
Write 0
Write 1
Read Circuit
16b
SA
Write Circuit
15n
Write 0
Write 1
Read Circuit
16n
SA
Sub-array 0
Column 0~(m-1)
17a
Sub-array 1
Column m~(2m-1)
17b
Sub-array n
Column (n-1)m ~(nxm-1)
17n
Row Decoder
19
N

FIGURE 1

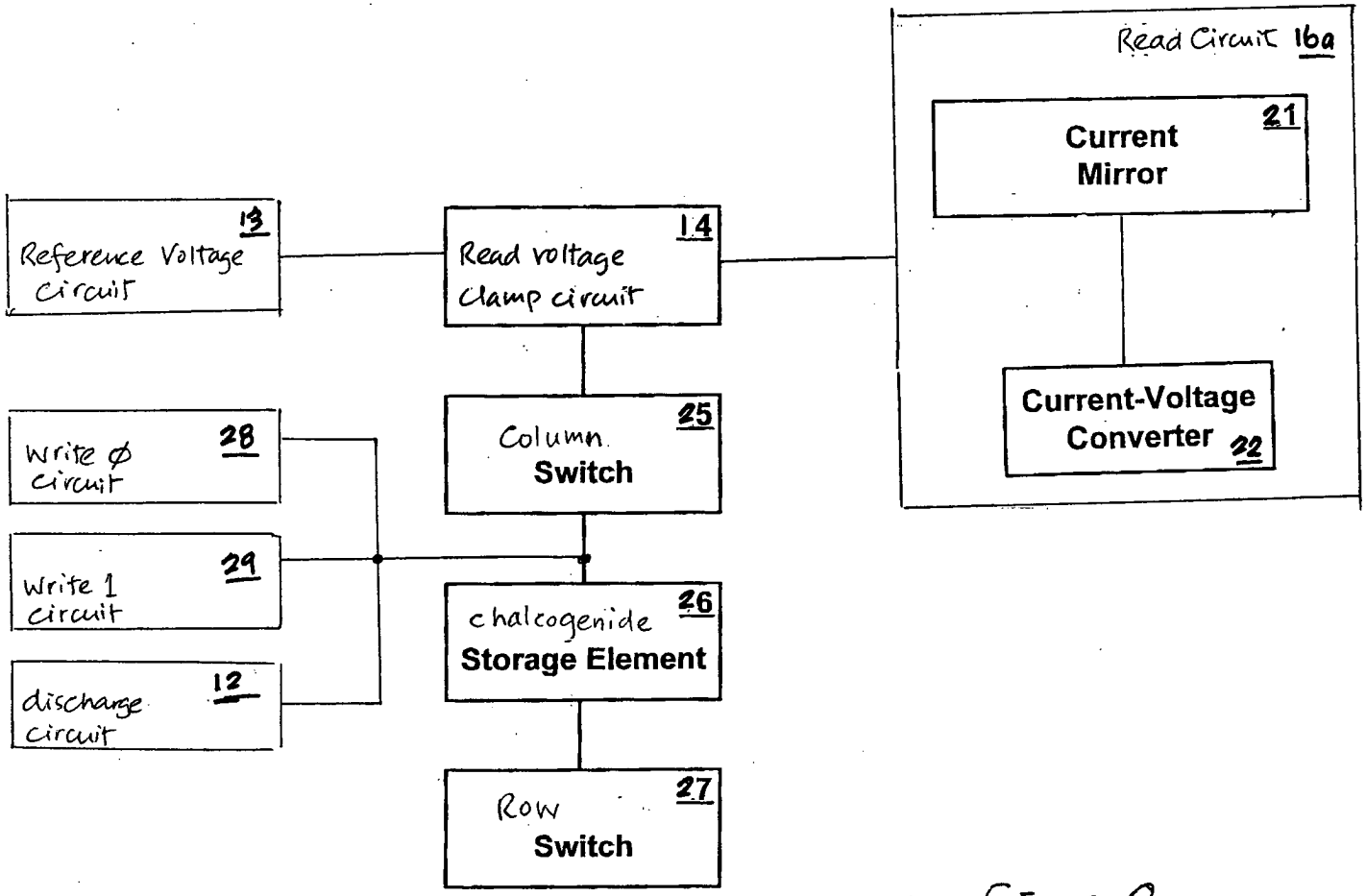
Read Circuit 16a
21
Current Mirror
Current-Voltage Converter 22
13
Reference Voltage circuit
14
Read voltage clamp circuit
25
Column Switch
28
Write ∅ circuit
29
Write 1 circuit
12
discharge circuit
26
chalcogenide Storage Element
27
Row Switch

FIGURE 2

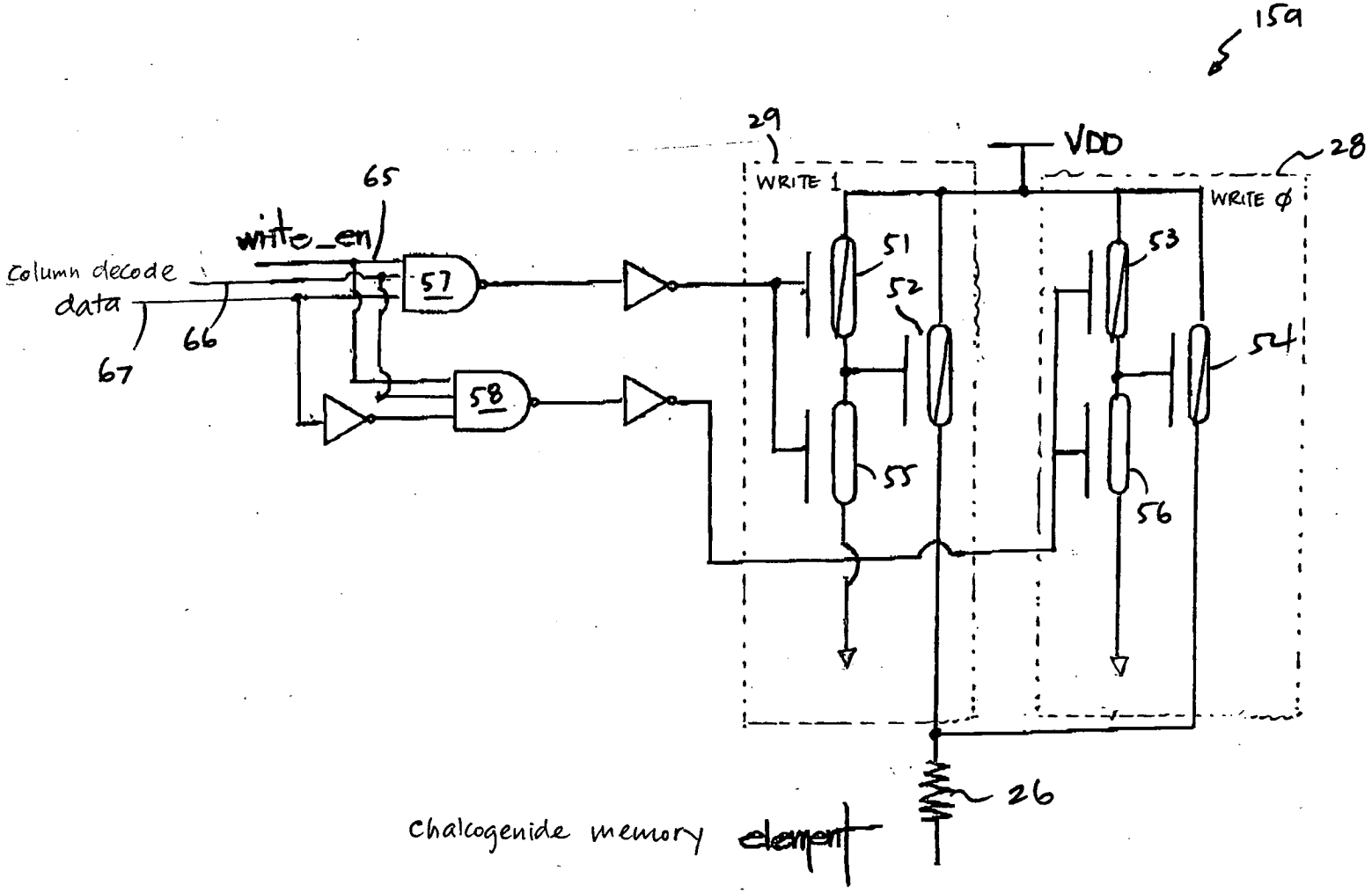
159
29
VDD
28
WRITE 1
WRITE ϕ
65
write_en
Column decode
data
66
67
57
58
51
52
53
54
55
56
26
Chalcogenide memory element

FIGURE 3

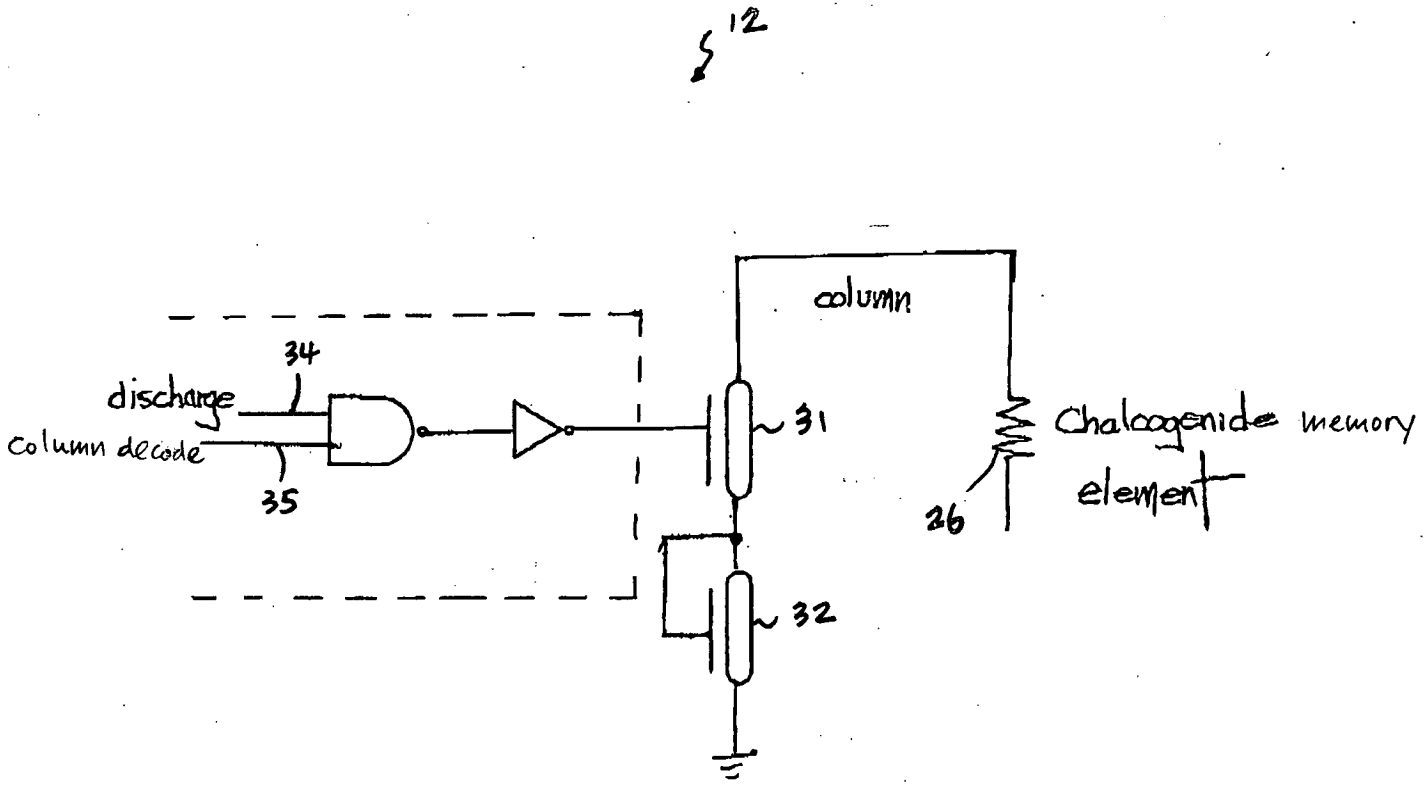
12
column
34
discharge
column decode
35
31
32
26
Chalcogenide memory
element

FIGURE 4

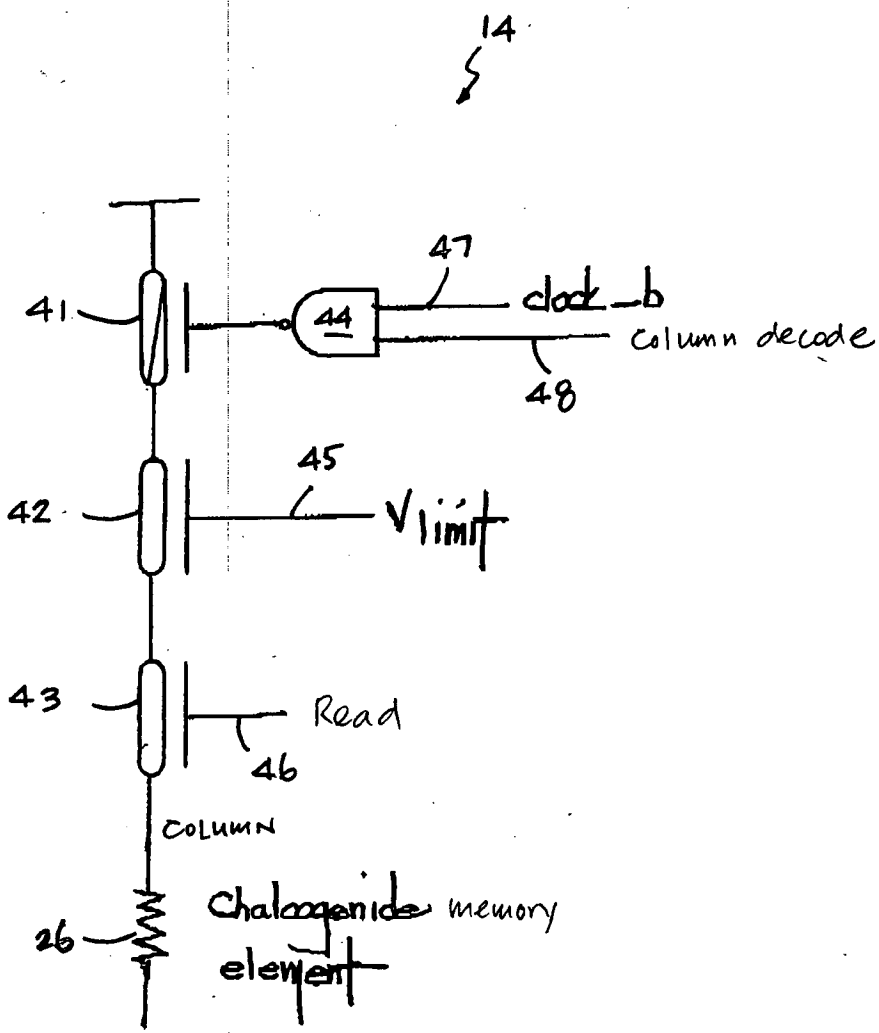
14
41
47
clock_b
44
column decode
48
45
42
Vlimit
43
Read
46
COLUMN
26
Chalcogenide memory
element

FIGURE 5